FULL-SIZE DIP HIGH-FREQUENCY CRYSTAL OSCILLATOR

SG-51 series

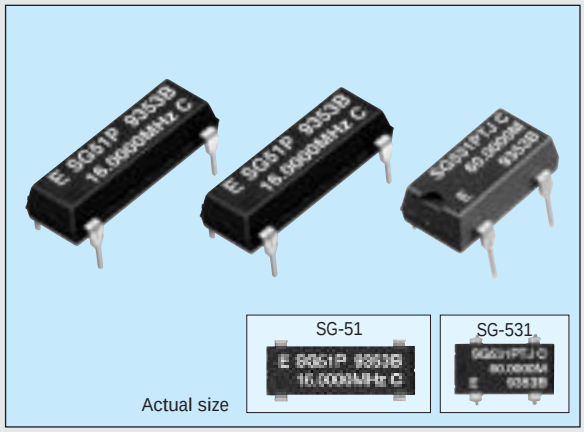
HALF-SIZE DIP HIGH-FREQUENCY CRYSTAL OSCILLATOR

SG-531 series

Product number (please refer to page 1)

Q32510xxxxxxx00
Q32531xxxxxxx00

- Pin compatible with full-size metal can. (SG-51 series)
- Pin compatible with half-size metal can. (SG-531 series)
- Cylindrical AT-cut crystal unit builtin, thus assuring high reliability.
- Use of CMOS IC enables reduction of current consumption.



Specifications (characteristics)

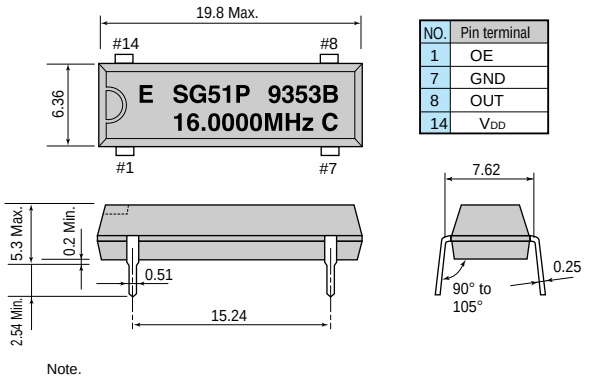
Item		Symbol	Specifications			Remarks
			SG-51P/531P	SG-51PTJ/531PTJ	SG-51PH/531PH	
Output frequency range		f_0	1.0250 MHz to 26.0000 MHz	26.0001 MHz to 66.6667 MHz		Refer to page 31. "Frequency range"
Power source voltage	Max. supply voltage	V_{DD}-GND		-0.3 V to +7.0 V	-0.5 V to +7.0 V	
	Operating voltage	V_{DD}		5.0 V±0.5 V		
Temperature range	Storage temperature	T_{STG}		-55 °C to +125 °C		Stored as bare product after unpacking
	Operating temperature	T_{OPR}	-20 °C to +70 °C (-40 °C to +85 °C)			Refer to page 31. "Frequency range"
Frequency stability		$\Delta f/f_0$		B: ± 50 x 10^{-6} C: ±100 x 10^{-6}		B type is possible up to 55.0 MHz
Current consumption		Iop	23 mA Max.	35 mA Max.		No load condition
Output disable current		I_{OE}	12 mA Max.	28 mA Max.	20 mA Max.	OE=GND
Duty	CMOS level	t_w/t	40 % to 60 %	—	40 % to 60 %	1/2 V_{DD} level
	TTL level		45 % to 55 %		—	1.4 V level
Output voltage		V_{OH}	V_{DD}-0.4 V Min.	2.4 V Min.	V_{DD} -0.4 V Min.	I_{OH} = -400 µA (P,PTJ) /-4 mA (PH)
		V_{OL}		0.4 V Max.		I_{OL} = 16 mA (P) / 8 mA (PTJ) / 4mA (PH)
Output load condition (fan out)	CMOS	C_L	50 pF Max.	—	50 pF Max.	
	TTL	N	10 TTL Max.	5 TTL Max.	—	C_L≤15 pF
Output enable/disable input voltage		V_{IH}	2.0 V Min.	3.5 V Min.	2.0 V Min.	I_{IH}=1 µA Max. (OE=V_{DD})
		V_{IL}	0.8 V Max.	1.5 V Max.	0.8 V Max.	I_{IL}= -100 µA Min. (OE=GND), PTJ: I_{IL} = -500 µA Min. (OE=GND)
Output rise time	CMOS level	t_{TLH}	8 ns Max.	—	7 ns Max.	CMOS load: 20 %→80 % V_{DD}
	TTL level			5 ns Max.	—	TTL load: 0.4 V→2.4 V
Output fall time	CMOS level	t_{THL}	8 ns Max.	—	7 ns Max.	CMOS load: 80 %→20 % V_{DD}
	TTL level			5 ns Max.	—	TTL load: 2.4 V→0.4 V
Oscillation start up time		t_{OSC}	4 ms Max.	10 ms Max.		More than for 1 ms until V_{DD} =0 V→4.5 V Time at 4.5 V to be 0 s
Aging		fa		±5 x 10^{-6}/year Max.		Ta=+25 °C, V_{DD} =5 V,first year
Shock resistance		S.R.		±20 x 10^{-6} Max.		Three drops on a hard board from 750 mm or excitation test with 29400 m/s² x 0.3 ms x 1/2 sine wave in 3 directions

Note: • Unless otherwise stated, characteristics (specifications) shown in the above table are based on the rated operating temperature and voltage condition.
• External by-pass capacitor is recommended.

External dimensions

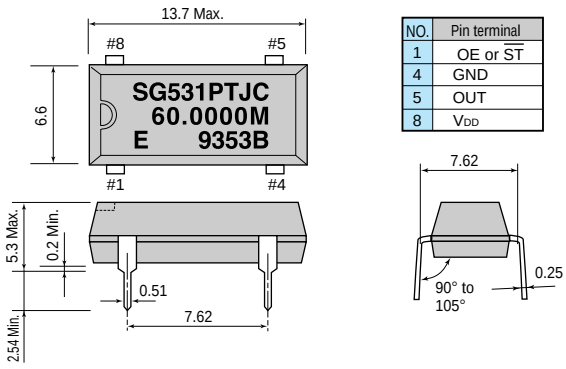
(Unit: mm)

SG-51 series



NO.	Pin terminal
1	OE
7	GND
8	OUT
14	V_{DD}

SG-531 series



NO.	Pin terminal
1	OE or $\overline{ST}$
4	GND
5	OUT
8	V_{DD}

Note.
OE Pin (P, PTJ, PH, PTW, PHW, PCW)
OE pin - "H" or "open" : Specified frequency output.
OE pin - "L" : Output is high impedance.

ST pin (STW, SHW, SCW)
ST pin - "H" or "open" : Specified frequency output.
ST pin - "L" : Output is low level (weak pull - down), oscillation stops.

Specifications (characteristics)

Item		Symbol	Specifications		Remarks
			SG-531PCG	SG-531SCG	
Output frequency range		f_O	1.5000 MHz to 26.0000 MHz		Refer to page 31. "Frequency range"
Power source voltage	Max. supply voltage	V_{DD}-GND	-0.5 V to +7.0 V		
	Operating voltage	V_{DD}	2.7 V to 3.6 V		
Temperature range	Storage temperature	T_{STG}	-55 °C to +125 °C		Stored as bare product after unpacking
	Operating temperature	T_{OPR}	-40 °C to +85 °C		Refer to page 31. "Frequency range"
Frequency stability		$\Delta f/f_0$	B : ±50 x 10^{-6} C : ±100 x 10^{-6}		-20 °C to +70 °C
			M : ±100 x 10^{-6}		-40 °C to +85 °C
Current consumption		I_{OP}	12 mA Max.		No load condition
Output disable current		I_{OE}	10 mA Max.	—	OE=GND (PCG)
Standby current		I_{ST}	—	50 µA Max.	ST=GND (SCG)
Duty		tw/t	45 % to 55 %		50 % V_{DD}, CL = 25 pF
Output voltage		V_{OH}	V_{DD} -0.4 V Min.		I_{OH} = -8 mA
		V_{OL}	0.4 V Max.		I_{OL} = 8 mA
Output load condition (fan out)		CL	25 pF		
Output enable disable input voltage		V_{IH}	70 % V_{DD} Min.		OE, $\overline{ST}$
		V_{IL}	20 % V_{DD} Max.		OE, $\overline{ST}$
Output rise time		t_{TLH}	4.0 ns Max.		20 % to 80 % V_{DD}, CL ≤ 25 pF
Output fall time		t_{THL}	4.0 ns Max.		80 % to 20 % V_{DD} CL ≤ 25 pF
Oscillation start up time		t_{OSC}	12 ms Max.		Time at minimum operating voltage to be 0 s
Aging		fa	±5 x 10^{-6} / year Max.		Ta=+25 °C, V_{DD} =3.3 V, First year
Shock resistance		S.R.	±20 x 10^{-6} Max.		Three drops on a hard board from 750 mm or excitation test with 29400 m/s2 x 0.3 ms x 1/2 sine wave in 3 directions

Specifications (characteristics)

Item		Symbol	Specifications			Remarks
			SG-531PTW/STW	SG-531PHW/SHW	SG-531PCW/SCW	
Output frequency range		f_O	55.0001 MHz to 135.0000 MHz		26.0001 MHz to 135.0000 MHz	Refer to page 31. "Frequency range"
Power source voltage	Max. supply voltage	V_{DD}-GND	-0.5 V to +7.0 V			
	Operating voltage	V_{DD}	5.0 V ± 0.5 V		3.3 V ± 0.3 V	
Temperature range	Storage temperature	T_{STG}	-55 °C to +100 °C			Stored as bare product after unpacking
	Operating temperature	T_{OPR}	-20 °C to +70 °C		-40 °C to +85 °C	Refer to page 31. "Frequency range"
Frequency stability		$\Delta f/f_0$	B : ±50 x 10^{-6} C : ±100 x 10^{-6}			-20 °C to +70 °C
			—		M : ±100 x 10^{-6}	-40 °C to +80 °C
Current consumption		I_{OP}	45 mA Max.		28 mA Max.	No load condition
Output disable current		I_{OE}	30 mA Max.		16 mA Max.	OE=GND(P*W)
Standby current		I_{ST}	50 µA Max.			$\overline{ST}$=GND(S*W)
Duty		tw/t	40 % to 60 %	—	—	TTL load : 1.4 V, CL = Max.
			45 % to 55 %	—	—	TTL load : 1.4 V, 5TTL + 15 pF, fo ≤ 66.6667 MHz
			—	40 % to 60 %	40 % to 60 %	CMOS load : 50% V_{DD}, CL = Max.
			—	45 % to 55%	—	CMOS load : 50% V_{DD}, CL = 25 pF, fo ≤ 66.6667 MHz
			—	—	45 % to 55%	CMOS load : 50% V_{DD}, CL = 25 pF, fo ≤ 40.0 MHz
Output voltage		V_{OH}	V_{DD} -0.4 V Min.			I_{OH}= -16 mA (*TW/*HW)/-8 mA(*CW)
		V_{OL}	0.4 V Max.			I_{OL}= 16 mA (*TW/*HW)/8 mA(*CW)
Output load condition (fan out)		CL	15 pF	—	—	fo ≤ 135 MHz
			5 TTL + 15 pF	—	—	fo ≤ 90 MHz
			25 pF	—	—	fo ≤ 66.6667 MHz
			—	15 pF	15 pF	fo ≤ 135 MHz
			—	25 pF	—	fo ≤ 125 MHz
			—	50 pF	—	fo ≤ 66.6667MHz
			—	—	30 pF	fo ≤ 40.0 MHz
Output enable disable input voltage		V_{IH}	2.0 V Min.		0.7 V_{DD} Min.	OE,$\overline{ST}$
		V_{IL}	0.8 V Max.		0.2 V_{DD} Max.	OE,$\overline{ST}$
Output rise time		t_{TLH}	2.0 ns Max.	—	—	TTL load: 0.8 V→2.0 V, CL = Max.
			4.0 ns Max.	—	—	TTL load: 0.4 V→2.4 V, CL = Max.
			—	3.0 ns Max.	—	CMOS load: 20 %→80 % V_{DD}, CL= 25 pF
			—	—	3.0 ns Max.	CMOS load: 20 %→80 % V_{DD}, CL= 15 pF
			—	4.0 ns Max.	4.0 ns Max.	CMOS load: 20 %→80 % V_{DD}, CL= Max.
Output fall time		t_{THL}	2.0 ns Max.	—	—	TTL load: 2.0 V→0.8 V, CL = Max.
			4.0 ns Max.	—	—	TTL load: 2.4 V→0.4 V, CL = Max.
			—	3.0 ns Max.	—	CMOS load: 80 %→20 % V_{DD}, CL= 25 pF
			—	—	3.0 ns Max.	CMOS load: 80 %→20 % V_{DD}, CL= 15 pF
			—	4.0 ns Max.	4.0 ns Max.	CMOS load: 80 %→20 % V_{DD}, CL= Max.
Oscillation start up time		t_{OSC}	10 ms Max.			Time at minimum operating voltage to be 0 s
Aging		fa	±5 x 10^{-6} /year Max.			Ta=+25 °C, VDD =5.0 V / 3.3 V, First year
Shock resistance		S.R.	±20 x 10^{-6} Max.			Three drops on a hard board from 750 mm or excitation test with 29400 m/s2 x 0.3 ms x 1/2 sine wave in 3 directions