General Description

The YQ2G6965 is a programmable clock generator intended for high-performance consumer, networking, industrial, computing, and data-communication applications. Configurations may be stored in on-chip efuse or changed using I2C interface. The device may be configured to use one of two I2C addresses to allow multiple devices to be used in a system.

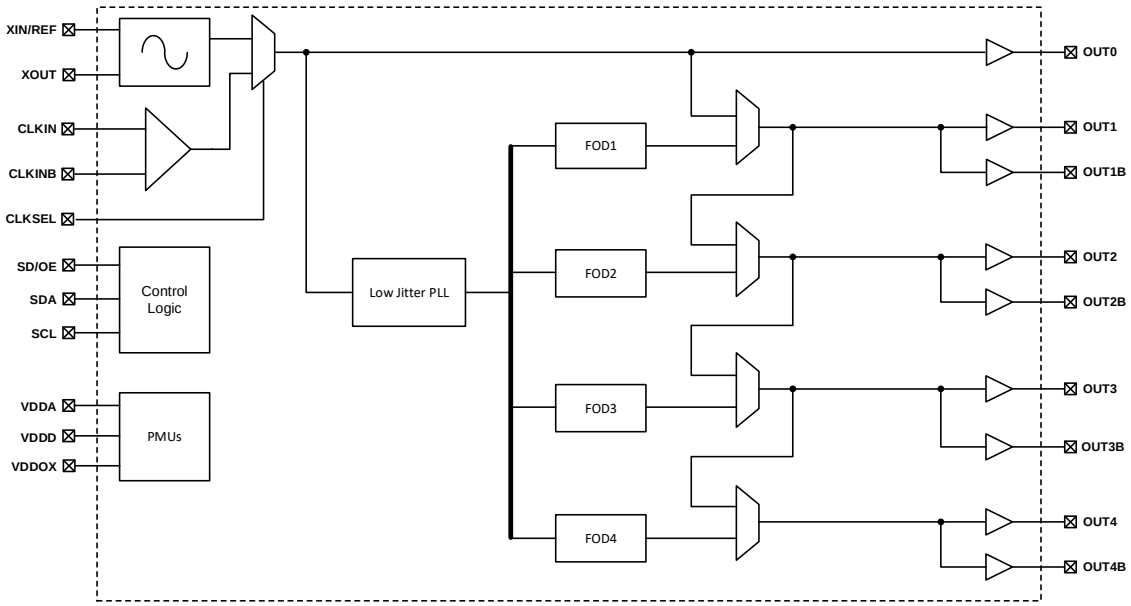
Applications

- Ethernet switch/router
- PCI Express 1.0/2.0/3.0/4.0/5.0/6.0 Spread Spectrum on
- Broadcast video/audio timing
- Multi-function printer
- Processor and FPGA clocking
- Any-frequency clock conversion
- MSAN/DSLAM/PON
- Fiber Channel, SAN
- Telecom line cards
- 1 GbE and 10 GbE

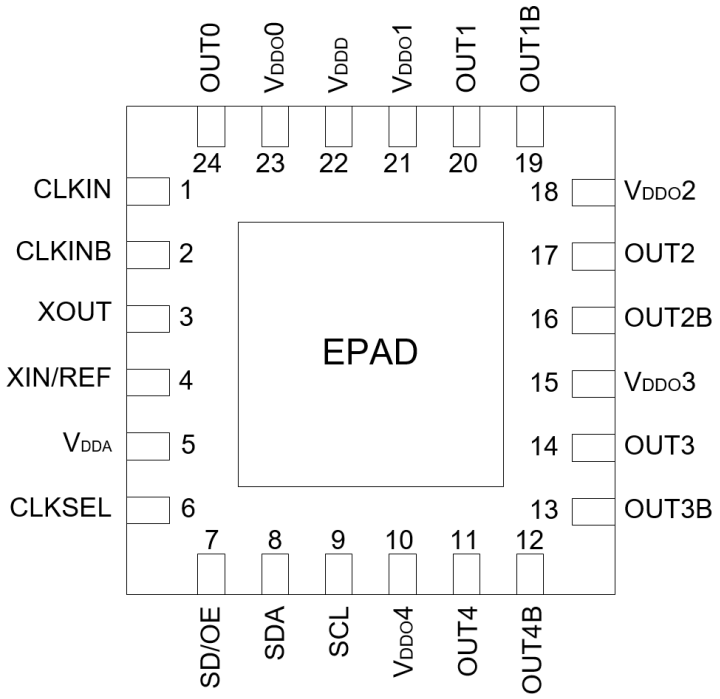
Features

- Flexible 1.8V, 2.5V, 3.3V power-rails
- High-performance, low phase noise PLL, < 0.5ps RMS typical phase jitter on outputs
- Reference LVCMOS output clock
- Four universal output pairs individually configurable:
  - Differential (LVPECL, LVDS or HCSL)
  - 2 single-ended (2 LVCMOS in-phase or 180 degrees out of phase)
- I/O VDDs can be mixed and matched, supporting 1.8V(LVDS and LVCMOS), 2.5V, or 3.3V
- Redundant clock inputs with manual switchover
- Input frequency range:
  - Crystal frequency range: 8MHz to 100MHz
- Output frequency ranges:
  - LVCMOS Clock Outputs – 1MHz to 200MHz
  - LP-HCSL Clock Outputs – 1MHz to 200MHz
  - Other Differential Clock Outputs – 1MHz to 300MHz
- Programmable crystal load capacitance
- Power-down mode
- I2C serial programming interface
- Available in 4 × 4 mm 24-pin QFN package
- -40° to +85°C industrial temperature operation applications

Functional Block Diagram



Pin Configuration



4 X 4 mm 24-QFN

Pin Functions

Table 1. Pin Descriptions

Number	Name	Type	Description
1	CLKIN	Input	Differential clock input. Weak 200kΩ internal pull-down.
2	CLKINB	Input	Complementary differential clock input. Weak 200kΩ internal pull-down.
3	XOUT	Output	Crystal oscillator interface output.
4	XIN/REF	Input	Crystal oscillator interface input, or single-ended LVCMOS clock input. Input voltage needs to be below 1.8V.
5	VDDA	Power	Analog functions power supply pin. Connect to 1.8V to 3.3V. VDDA and VDDD should have the same voltage applied.
6	CLKSEL	Input	Input clock select. Selects the active input reference source in manual switchover mode. 0 = XIN/REF, XOUT (default). 1 = CLKIN, CLKINB.
7	SD/OE	Input	Enables/disables the outputs (OE) or powers down the chip (SD).
8	SDA	Input	I2C SDA input.
9	SCL	Input	I2C SCL input.
10	VDDO4	Power	Output power supply. Connect to 1.8 to 3.3V. Sets output voltage levels for OUT4/OUT4B.
11	OUT4	Output	Output clock 4.
12	OUT4B	Output	Complementary output clock 4.
13	OUT3B	Output	Complementary output clock 3.
14	OUT3	Output	Output clock 3.
15	VDDO3	Power	Output power supply. Connect to 1.8 to 3.3V. Sets output voltage levels for OUT3/OUT3B.

16	OUT2B	Output	Complementary output clock 2.
17	OUT2	Output	Output clock 2.
18	VDDO2	Power	Output power supply. Connect to 1.8 to 3.3V. Sets output voltage levels for OUT2/OUT2B.
19	OUT1B	Output	Complementary output clock 1.
20	OUT1	Output	Output clock 1.
21	VDDO1	Power	Output power supply. Connect to 1.8 to 3.3V. Sets output voltage levels for OUT1/OUT1B.
22	VDDD	Power	Connect to 1.8 to 3.3V. VDDA and VDDD should have the same voltage applied.
23	VDDO0	Power	Power supply pin for OUT0. Connect to 1.8 to 3.3V. Sets output voltage levels for OUT0.
24	OUT0	Output	Output clock 0, the pin acts as a LVCMOS reference output.
25	GND	GND	Connect to ground pad.

Features and Functional Blocks

Device Startup and Power-On-Reset

The device has an internal power-up reset (POR) circuit. All VDDs must be connected to desired supply voltage to trigger POR.

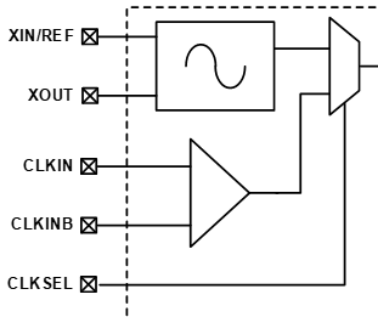
User can define specific default configurations through internal efuse memory. Either customer or factory can program the default configuration. Please refer to Register Descriptions and Programming Guide for details or contact Renesas if a specific factory-programmed default configuration is required.

Reference Clock and Selection

The device supports up to two clock inputs.

- Crystal input, can be driven by a single-ended clock.
- Clock input (CLKIN, CLKINB), a fully differential input that only accepts a reference clock. A single-ended clock can also drive it on CLKIN.

Figure 7. Clock Input Diagram, Internal Logic



CLKSEL
0 = XIN/REF, XOUT (default).
1 = CLKIN, CLKINB.

Internal Crystal Oscillator (XIN/REF)

Choosing Crystals

A crystal manufacturer will calibrate its crystals to the nominal frequency with a certain load capacitance value. When the oscillator load capacitance matches the crystal load capacitance, the oscillation frequency will be accurate. When the oscillator load capacitance is lower than the crystal load capacitance, the oscillation frequency will be higher than nominal and vice versa so for an accurate oscillation frequency you need to make sure to match the oscillator load capacitance with the crystal load capacitance. To set the oscillator load capacitance there are two tuning capacitors in the IC, one at XIN and one at XOUT. They can be adjusted independently but commonly the same value is used for both capacitors. The value of each capacitor is composed of a fixed capacitance amount plus a variable capacitance amount set with the XTAL[5:0] register. Adjustment of the crystal tuning capacitors allows for maximum flexibility to accommodate crystals from various manufacturers. The range of tuning capacitor values available are in accordance with the following table.

XTAL[5:0] Tuning Capacitor Characteristics

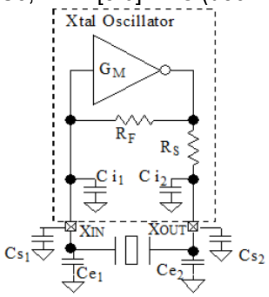
Parameter	Bits	Step (pF)	Min (pF)	Max (pF)
XTAL	6	0.3	6	25

The capacitance at each crystal pin inside the chip starts at 6pF with setting 000000b and can be increased up to 25pF with setting 111111b. The step per bit is 0.3pF.
You can write the following equation for this capacitance:
Ci = 6pF + 0.3pF × XTAL[5:0]

Tuning the Crystal Load Capacitor

Cs1 and Cs2 are stray capacitances at each crystal pin and typical values are between 1pF and 3pF.
Ce1 and Ce2 are additional external capacitors, increasing the load capacitance reduces the oscillator gain so please consult the factory when adding Ce1 and/or Ce2 to avoid crystal startup issues.

You can write the following equation for this capacitance:
CXIN = Ci1 + Cs1 + Ce1
CXOUT = Ci2 + Cs2 + Ce2
The final load capacitance of the crystal:
CL = CXIN × CXOUT / (CXIN + CXOUT)
It is recommended to set the same value for capacitors the same at each crystal pin, meaning:
CXIN = CXOUT
The complete formula when the capacitance at both crystal pins is the same:
CL = (6pF + 0.3pF × XTAL[5:0] + Cs + Ce) / 2
Example 1: The crystal load capacitance is specified as 7.5pF and the stray capacitance at each crystal pin is Cs = 1.5pF. Assuming equal capacitance value at XIN and XOUT, the equation is as follows:
7.5pF = (6pF + 0.3pF × XTAL[5:0] + 1.5pF) / 2
So, XTAL[5:0] = 25 (decimal).



Fractional Output Dividers (FOD)

Spread Spectrum

To help reduce electromagnetic interference (EMI), the YQ2G6965 supports spread spectrum modulation. The output clock frequencies can be modulated to spread energy across a broader range of frequencies, lowering system EMI. The YQ2G6965 implements spread spectrum using the Fractional-N output divide, to achieve controllable modulation
rate and spreading magnitude. The Spread spectrum can be applied to any output divider and any spread amount from ±0.1% to ±3% center spread and -0.5% to -6% down spread.

Programmable Loop Filter

Table 2. Loop Filter

PLL loop bandwidth range depends on the input reference frequency (Fref) and can be set between the loop bandwidth range as shown in the table below.

Input Reference Frequency–Fref (MHz)	Loop Bandwidth Min (kHz)	Loop Bandwidth Max (kHz)
8	50	200
350	300	1000

Output Drivers

The device output drivers support the following features individually:

▪ The outputs are provided with register-controlled output drivers.
▪ 2.5V or 3.3V voltage level for HCSL/LVPECL operation
▪ 1.8V, 2.5V or 3.3V voltage levels for CMOS/LVDS operation
▪ CMOS supports 4 operating modes:
• CMOSD: OUTx and OUTxB 180 degrees out of phase
• CMOSX2: OUTx and OUTxB phase-aligned
• CMOS1: only OUTx pin is on
• CMOS2: only OUTxB pin is on

When a given output is configured to at CMOSD or CMOSX2, then all previously described configuration and control apply equally to both pins.

▪ Independent output enable/disabled by register bits. When
disabled, an output can be either in a logic 1 state or Hi-Z.

The following options are used to disable outputs:

1. Output turned off by I2C.
2. Output turned off by SD/OE pin.
3. Output unused, which means is turned off regardless of OE pin status.

SD/OE Pin Function

SH bit	SP bit	OSn bit	OEn bit	SD/OE	OUTn
0	0	0	x	x	Tri-state
0	0	1	0	x	Output active
0	0	1	1	0	Output active
0	0	1	1	1	Output driven High Low
0	1	0	x	x	Tri-state
0	1	1	0	x	Output active
0	1	1	1	0	Output driven High Low
0	1	1	1	1	Output active
1	0	0	x	0	Tri-state
1	0	1	0	0	Output active
1	0	1	1	0	Output active
1	1	0	x	0	Tri-state
1	1	1	0	0	Output active
1	1	1	1	0	Output driven High Low
1	x	x	x	1	Output driven High Low

Note 1: Global Shutdown Note 2: Tri-state regardless of OEn bits

Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the device at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Item	Rating
Supply Voltage, V_{DDA}, V_{DDD}, V_{DDOX}	3.465V
Inputs XIN/REF	0V to 1.8V voltage swing
Package Thermal Impedance, Θ_{JA}	42°C/W (0 mps)
Package Thermal Impedance, Θ_{JC}	41.8°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C
ESD Human Body Model	2000V
Junction Temperature	125°C

Thermal Characteristics

Table 4. Thermal Characteristics

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDDOX	Power supply voltage for supporting 1.8V outputs.	1.71	1.8	1.89	V
	Power supply voltage for supporting 2.5V outputs.	2.375	2.5	2.625	V
	Power supply voltage for supporting 3.3V outputs.	3.135	3.3	3.465	V
VDDD	Power supply voltage for core logic functions.	1.75		3.465	V
VDDA	Analog power supply voltage. Use filtered analog power supply.	1.75		3.465	V
TA	Operating temperature, ambient	-40		85	°C
CLOAD_OUT	Maximum load capacitance (3.3V LVCMOS only)			15	pF
FIN	External reference crystal	8		100	MHz
tPU	Power up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic)	0.05		5	ms

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		8	25	100	MHz
Equivalent Series Resistance (ESR) < 50 MHz			10	100	Ω
Equivalent Series Resistance (ESR) >= 50 MHz			10	25	Ω
Shunt Capacitance				7	pF
Load Capacitance (CL) <=25 MHz		6	8	12	pF
Load Capacitance (CL) >25M		6		8	pF
Maximum Crystal Drive Level <=25 MHz				100	µW
Maximum Crystal Drive Level >25M to 50MHz				200	µW
Maximum Crystal Drive Level >50M to 100MHz				300	µW

Electrical Characteristics

Table 6. Current Consumption

symbol	Parameter	Test Conditions		Typ	Max	Unit
Iddcore[3]	Core Supply Current	100 MHz on all outputs, 25 MHz REFCLK	1.8V	85		mA
			2.5V	92		mA
			3.3V	92		mA
		LVPECL, 300MHz, 3.3V VDDOx		31	34.1	mA
		LVPECL, 300MHz, 2.5V VDDOx		29	31.9	mA
		LVDS, 300MHz, 3.3V VDDOx		10	11	mA
		LVDS, 300MHz, 2.5V VDDOx		10	11	mA
		LVDS, 300MHz, 1.8V VDDOx		9	9.9	mA
		HCSL, 250MHz, 3.3V VDDOx, 2pF load		21	23.1	mA
		HCSL, 250MHz, 2.5V VDDOx, 2pF load		22	24.2	mA
		LVCMOS, 50MHz, 3.3V, VDDOx[1,2]		12		mA
		LVCMOS, 50MHz, 2.5V, VDDOx[1,2]		9		mA
		LVCMOS, 50MHz, 1.8V, VDDOx[1,2]		6		mA
		LVCMOS, 200MHz, 3.3V VDDOx[1]		4		mA
		LVCMOS, 200MHz, 2.5V VDDOx[1,2]		2		mA
		LVCMOS, 200MHz, 1.8V VDDOx[1,2]		2		mA
Iddpd	Power Down Current	SD asserted, I2C Programming	1.8V	8		mA
			2.5V	9		mA
			3.3V	9		mA

1. Single CMOS driver active.

2. Measured into a 5” 50 Ohm trace with 2 pF load.

3. Iddcore = IddA+ IddD, no loads

Table 7. AC Timing Characteristics

(VDDA, VDDD, VDDO1234 = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, TA = -40°C to +85°C unless stated otherwise.)

(Spread Spectrum Generation = OFF)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Fin	Input Frequency	Input frequency limit (crystal).	8		100	MHz
		Input frequency limit (CLKIN, CLKINB).	8		200	MHz
		Input frequency limit (single-ended over XIN).	8		200	MHz
Fout	Output Frequency	Single ended clock output limit (LVCMOS)	1		200	MHz
		Differential clock output limit	1		300	MHz
FVCO	VCO Frequency	VCO operating frequency range	2100		2400	MHz
			1950		2250	MHz
FPFD	PFD Frequency	PFD operating frequency range	8		100	MHz
FBW	Loop Bandwidth	Input frequency = 25MHz	0.06		0.9	MHz
t2	Input Duty Cycle	Duty Cycle	45		55	%
t3 [5]	Output Duty Cycle	Measured at VDD/2, all outputs except Reference output OUT0, VDDOX = 2.5V or 3.3V	45	50	55	%
		Measured at VDD/2, all outputs except Reference output OUT0, VDDOX=1.8V	40	50	60	%
		Measured at VDD/2, Reference output OUT0 (5MHz - 120MHz) with 50% duty cycle input	40	50	60	%
		Measured at VDD/2, Reference output OUT0 (150.1MHz - 200MHz) with 50% duty cycle input	30	50	70	%
t5	Rise Times	LVDS, 20% to 80%		300		ps
	Fall Times	LVDS, 80% to 20%		300		
	Rise Times	LVPECL, 20% to 80%		400		
	Fall Times	LVPECL, 80% to 20%		400		
t6	Clock Jitter	Cycle-to-Cycle jitter (Peak-to-Peak), multiple output frequencies switching, differential outputs		46		ps
		Cycle-to-Cycle jitter (Peak-to-Peak), multiple output frequencies switching, LVCMOS outputs		74		ps
		RMS Phase Jitter (12kHz to 5MHz integration range) reference clock (OUT0), 25 MHz LVCMOS outputs		0.1		ps

		RMS Phase Jitter (12kHz to 20MHz integration range) differential output, 25MHz crystal, 156.25MHz on OUT2, and 100MHz LP-HCSL outputs on OUT3, OUT5-11.		0.75	1.5	ps
t8 [3]	Startup Time	PLL lock time from power-up, measured after all VDD's have raised above 90% of their target value.		2	3	ms
t9 [4]	Startup Time	PLL lock time from shutdown mode		65	130	ms

1. Practical low er frequency is determined by loop filter settings.
2. A slew rate of 2.75V/ns or greater should be selected for output frequencies of 100MHz or higher.
3. Includes loading the configuration bits from efuse to PLL registers. It does not include efuse programming/write time.
4. Actual PLL lock time depends on the loop configuration.
5. Spread Spectrum generation is off unless otherwise stated.

Table 8. General Input Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
C_{IN}	Input Capacitance	SD/OE, SDA, SCL		3	7	pF
R_{PD}	Pull-down Resistor	SD/OE		200		kΩ
V_{IH}	XIN/REF		1.4		1.8	V
V_{IL}	XIN/REF		GND-0.3		0.4	V

Table 9 Electrical Characteristics – CMOS Outputs[1]

VDDA, VDDD, VDDO1234 = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, TA = -40°C to +85°C unless stated otherwise.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
R_{OUT}	Output Driver Impedance	CMOS output driver.		50		Ω

1. Guaranteed by design and characterization, not 100% tested in production.

Table 10. Electrical Characteristics – LVDS Outputs[1]

VDDA, VDDD, VDDO1234 = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, TA = -40°C to +85°C unless stated otherwise.

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{OT} (+)	Differential Output Voltage for the TRUE Binary State	280	400	440	mV
V_{OT} (-)	Differential Output Voltage for the FALSE Binary State	-440	-400	-280	mV
Δ V_{OT}	Change in V_{OT} between Complimentary Output States			60	mV
V_{OS}	Output Common Mode Voltage (Offset Voltage)	1.1	1.2	1.3	V
Δ V_{OS}	Change in V_{OS} between Complimentary Output States				mV
I_{OS}	Outputs Short Circuit Current, V_{OUT}+ or V_{OUT} - = 0V				
I_{OSD}	Differential Outputs Short Circuit Current, V_{OUT}+ = V_{OUT} -				
T_R	LVDS rise time 20%-80%		300		ps
T_F	LVDS fall time 80%-20%		300		ps

1. Guaranteed by design and characterization, not 100% tested in production.

Table 11. Electrical Characteristics – LVPECL Outputs[1]

VDDA, VDDD, VDDO1234 = 3.3V ±5%, 2.5V ±5%, TA = -40°C to +85°C unless stated otherwise.

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{OH}	Output Voltage High, Terminated through 50Ω tied to VDD -	2.2		2.8	mV

	2V				
V_{OL}	Output Voltage Low, Terminated through 50Ω tied to VDD - 2V	1.4		1.9	V
V_{SWING}	Peak-to-Peak Differential Output Voltage Swing	1.4		1.8	V
T_R	LVPECL rise time 20%–80%		300		ps
T_F	LVPECL fall time 80%–20%		300		ps

1. *Guaranteed by design and characterization, not 100% tested in production.*

Table 12. Electrical Characteristics – HCSL Outputs[1]

VDDA, VDDD, VDDO1234 = 3.3V ±5%, 2.5V ±5%, TA = -40°C to +85°C unless stated otherwise.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
dV/dt	Slew Rate	Scope averaging on [2, 3]		1.8		V/ns
Δ dV/dt	Slew Rate Matching	Scope averaging on [2, 3]		6		%
V_{MAX}	Maximum Voltage	Measurement on single-ended signal using absolute value (scope averaging off).			900	mV
V_{MIN}	Minimum Voltage		-30			mV
V_{SWING}	Voltage Swing	Scope averaging off [6]	500			mV
V_{CROSS}	Crossing Voltage Value	Scope averaging off [4, 6]	450		520	mV
Δ V_{CROSS}	Crossing Voltage Variation	Scope averaging off [5]				mV

1. *Guaranteed by design and characterization, not 100% tested in production.*
2. *Measured from differential waveform.*
3. *Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/- 150mV window around differential 0V.*
4. *Vcross is defined as voltage where Clock = Clock# measured on a component test board.*
5. *The total variation of all VCROSS measurements in any particular system.*
6. *Measured from single-ended waveform.*

Table 13. Spread Spectrum Generation Specifications

Symbol	Parameter	Description	Min	Typ	Max	Unit
f_{OUT}	Output Frequency	Output frequency range	1		140	MHz
f_{MOD}	Mod Frequency	Modulation frequency	20 to 100			kHz
f_{SPREAD}	Spread Value	Amount of spread value (programmable) - center spread	±0.1% to ±3%			%Fout
		Amount of spread value (programmable) - down spread	-0.5% to -6%			

Jitter Performance Characteristics

Figure 6. Typical Phase Jitter Plot at 100MHz

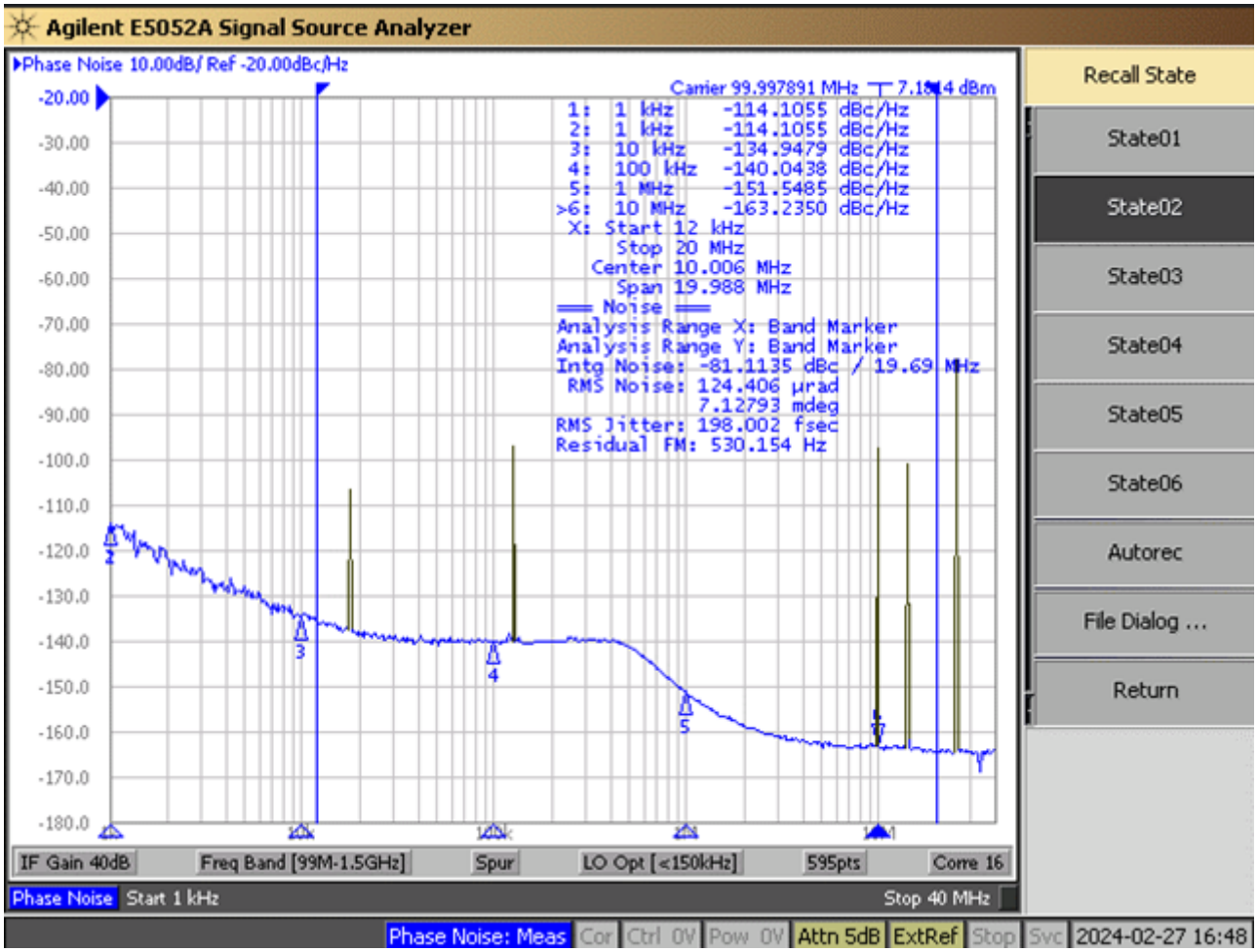


Table 14. Spread Spectrum Generation Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	PCIe Industry Specification	Units	Notes
tJ (PCIe Gen1)	Phase Jitter Peak to Peak	f = 100MHz, 25MHz crystal input evaluation band: 0Hz - Nyquist (clock frequency/2)				86	ps	1,4
tREFCLK_HF_RMS (PCIe Gen2)	Phase Jitter RMS	f = 100MHz, 25MHz crystal input high band: 1.5MHz - Nyquist (clock frequency/2)		0.3		3.1	ps	2,4
tREFCLK_LF_RMS (PCIe Gen2)	Phase Jitter RMS	f = 100MHz, 25MHz crystal input low band: 10kHz - 1.5MHz		0.03		3	ps	2,4
tREFCLK_RMS (PCIe Gen3)	Phase Jitter RMS	f = 100MHz, 25MHz crystal input evaluation band: 0Hz - Nyquist (clock frequency/2)		0.1		1	ps	3,4

Note: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

1. Peak-to-Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1.

2. RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each

evaluation band. Maximum limit for PCI Express Generation 2 is 3.1ps RMS for tREFCLK_HF_RMS (High Band) and 3.0ps RMS for tREFCLK_LF_RMS (Low Band).

3. RMS jitter after applying system transfer function for the common clock architecture. This specification is based on the PCI_Express_Base_r3.0 10 Nov, 2010 specification, and is subject to change pending the final release version of the specification.

Input – Driving the XIN/REF or CLKIN

Driving XIN/REF with a CMOS Driver

In some cases, it is encouraged to have XIN/REF driven by a clock input for reasons like better SNR, multiple input select with device CLKIN, etc. The XIN/REF pin is able to take an input when its amplitude is between 500mV and 1.8V and the slew rate more than 0.2V/ns.

The XIN/REF input can be driven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XOUT pin can be left floating.

Figure driving XIN with a CMOS Driver

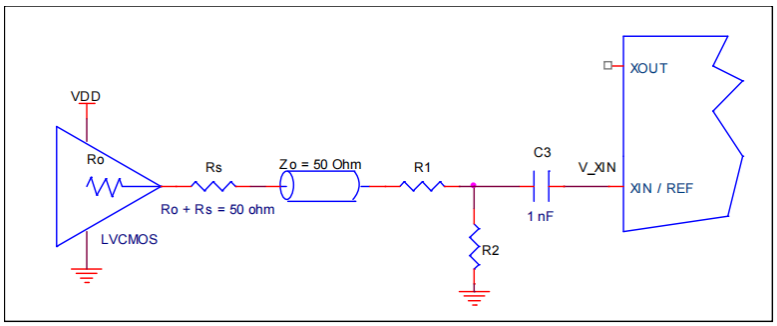


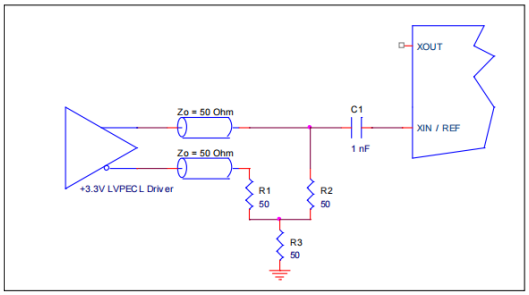
Table 15. Nominal Voltage Divider Values for driving XIN with Single-ended Driver

LVCMOS Driver V_{DD}	R_O+R_S	R1	R2	V_XIN (peak)	$R_O+R_S+R1+R2$
3.3	50.0	160	110	1.13	320
2.5	50.0	82	110	1.13	213
1.8	50.0	20	110	1.10	340

Driving XIN with an LVPECL Driver

Figure 1 shows an example of the interface diagram for a +3.3V LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XIN/REF input. It is recommended that all components in the schematics be placed in the layout; though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input. If the driver is 2.5V LVPECL, the only change necessary is to use the appropriate value of R3.

Figure 1. driving XIN with an LVPECL Driver



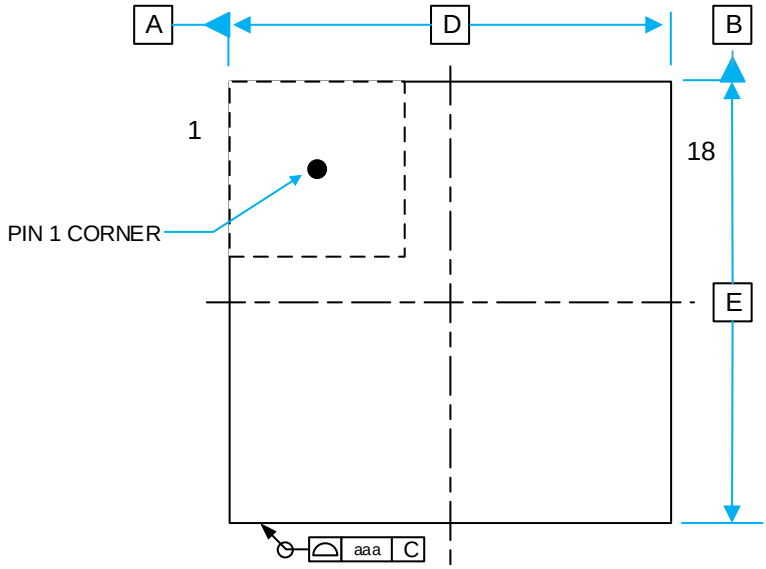
Order Information

Part No.	Package	Mark	Tape and Reel Information
YQ2G6965	QFN 4mmX4mm-24L	YQ2G6965	5000pcs/Reel

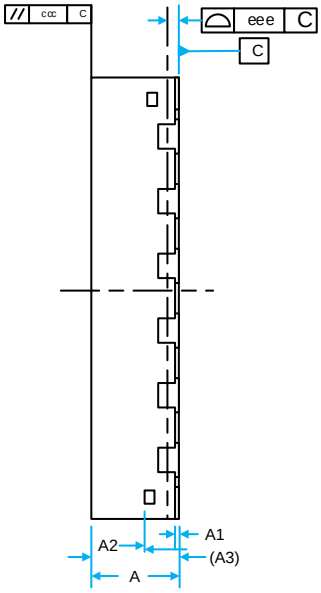
Package Outline

QFN 4mmX4mm-24L

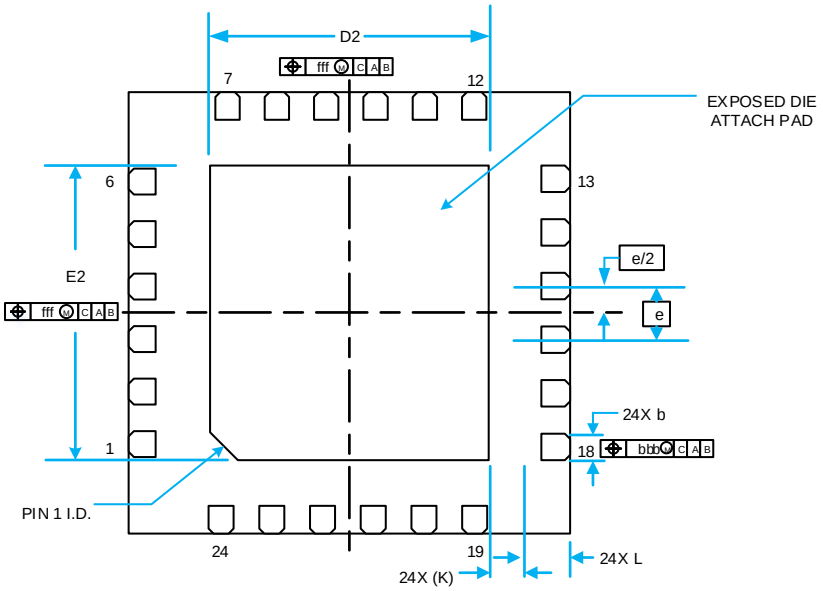
Quad Flat No-Lead Package, 24 leads. Body width 4mm, body length 4mm, body thickness 0.75mm, lead pitch 0.5mm.



TOP VIEW



SIDE VIEW



BOTTOM VIEW

COMMOV DIMENSIONS (UNITS OF MEASURE=MILLIMETER)					
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3	0.203 REF		
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D	4 BSC		
	Y	E	4 BSC		
LEAD PITCH		e	0.5 BSC		
EP SIZE	X	D2	2.7	2.8	2.9
	Y	E2	2.7	2.8	2.9
LEAD LENGTH		L	0.2	0.3	0.4
LEAD TIP TO EXPOSED PAD EDGE		K	0.3 REF		
PACKAGE EDGE TOLERANCE		aaa	0.1		
MOLD FLATNESS		ccc	0.1		
COPLANARITY		eee	0.08		
LEAD OFFSET		bbb	0.1		
EXPOSED PAD OFFSET		fff	0.1		

Revision History

No	Date	Description
V1.0	2024/04/09	First release
V1.3	2024/04/11	Modify power supply related info
V1.4	2024/04/12	Modify pin configuration