General Description

The YQ1S105 is a modular, high-performance, low additive jitter, low-skew, general-purpose clock buffer from YunQi. The entire family is designed with a modular approach in mind. It is intended to round up YunQi's series of LVCMOS clock generators.

All of the devices are pin-compatible to each other for easy handling.

The YQ1S105 family operates in a 1.8-V, 2.5-V and 3.3-V environment and are characterized for operation from –40°C to 85°C.

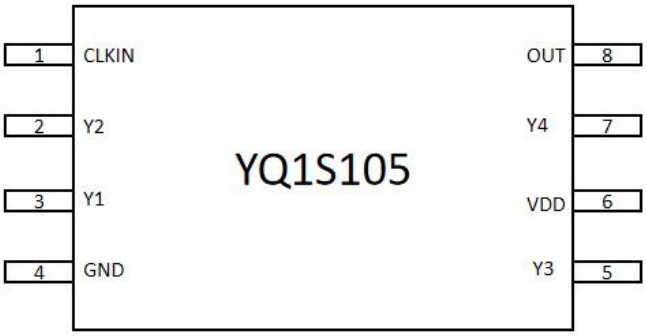
Features

- High-Performance 1:5 LVCMOS Clock Buffer
- Very Low Pin-to-Pin Skew < 50 ps
- Very Low Additive Jitter < 50 fs
- Supply Voltage: 1.8-V, 2.5-V or 3.3-V
  – fmax = 250 MHz for 3.3-V
  – fmax = 200 MHz for 2.5-V/1.8-V
- Operating Temperature Range: –40°C to 85°C
- Available in 8-Pin SOP Package (All Pin-Compatible)

Applications

➢ General-Purpose Communication, Industrial, and Consumer Applications

Pin Diagram



Pin Functions

Number	Name	Type	Description
1	CLKIN	Input	Input Clock Pin
2	Y2	Output	LVCMOS output.
3	Y1	Output	LVCMOS output.
4	GND	Ground	Ground
5	Y3	Output	LVCMOS output.
6	VDD	Power	Supply Voltage: 1.8-V, 2.5-V or 3.3-V
7	Y4	Output	LVCMOS output.
8	OUT	Output	LVCMOS output.

Specifications

Absolute Maximum Ratings

Item	Rating
Supply Voltage,VDD	3.465V
Inputs CLKIN/1G	-0.3V ~ VDD+ 0.3V
Storage Temperature, T_{STG}	-65°C to 150°C
ESD Human Body Model	4000V
Junction Temperature	125°C

Electrical Characteristics

(VDD = 3.3V ± 5%, TA = -40°C to +85°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
VDD	Power supply voltage for supporting 3.3V outputs		3.135	3.3	3.465	V
V_{IH}	High-level input voltage		0.7*VDD		1.05*VDD	
V_{IL}	Low-level output voltage				0.3*VDD	
V_{OH}	High-level output voltage	I_{OH} = –8 mA	2.5			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA			0.5	
I_{DD}	Supply Current	100MHz, CL=5pF		23		mA

(VDD = 2.5V ± 5%, TA = -40°C to +85°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
VDD	Power supply voltage for supporting 2.5V outputs.		2.375	2.5	2.625	V
V_{IH}	High-level input voltage		0.7*VDD		1.05*VDD	
V_{IL}	Low-level output voltage				0.3*VDD	
V_{OH}	High-level output voltage	I_{OH} = –8 mA	1.9			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA			0.5	
I_{DD}	Supply Current	100MHz		18		mA

(VDD = 1.8V ± 5%, TA = -40°C to +85°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
VDD	Power supply voltage for supporting 1.8V outputs.		1.71	1.8	1.89	V
V_{IH}	High-level input voltage		0.7*VDD		1.05*VDD	
V_{IL}	Low-level output voltage				0.3*VDD	
V_{OH}	High-level output voltage	I_{OH} = –8 mA	1.2			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA			0.5	
I_{DD}	Supply Current	100MHz		15		mA

AC Timing Characteristics

(VDD = 3.3V ± 5%, TA = -40°C to +85°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
fin	Input Frequency	Input frequency limit (XIN)	10^{-6}		250	MHz
T_{DC}	Input Duty Cycle	Duty Cycle	45		55	%
T_R	Rise Times	20% to 80%		350	1000	ps
T_F	Fall Times	80% to 20%		350	1000	
T_{jitter}	Additive Jitter	100MHz, 12kHz to 20MHz		15	30	fs
T_{sk_o}	Output to output skew				50	ps

(VDD = 2.5V ± 5%, TA = -40°C to +85°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
fin	Input Frequency	Input frequency limit (XIN)	10^{-6}		200	MHz
T_{DC}	Input Duty Cycle	Duty Cycle	45		55	%
T_R	Rise Times	20% to 80%		350	1000	ps
T_F	Fall Times	80% to 20%		350	1000	
T_{jitter}	Additive Jitter	100MHz, 12kHz to 20MHz		22	40	fs
T_{sk_o}	Output to output skew				50	ps

(VDD = 1.8V ± 5%, TA = -40°C to +85°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
fin	Input Frequency	Input frequency limit (XIN)	10^{-6}		200	MHz
T_{DC}	Input Duty Cycle	Duty Cycle	45		55	%
T_R	Rise Times	20% to 80%		400	1000	ps
T_F	Fall Times	80% to 20%		400	1000	
T_{jitter}	Additive Jitter	100MHz, 12kHz to 20MHz		50	80	fs
T_{sk_o}	Output to output skew				50	ps

Phase Noise Plot

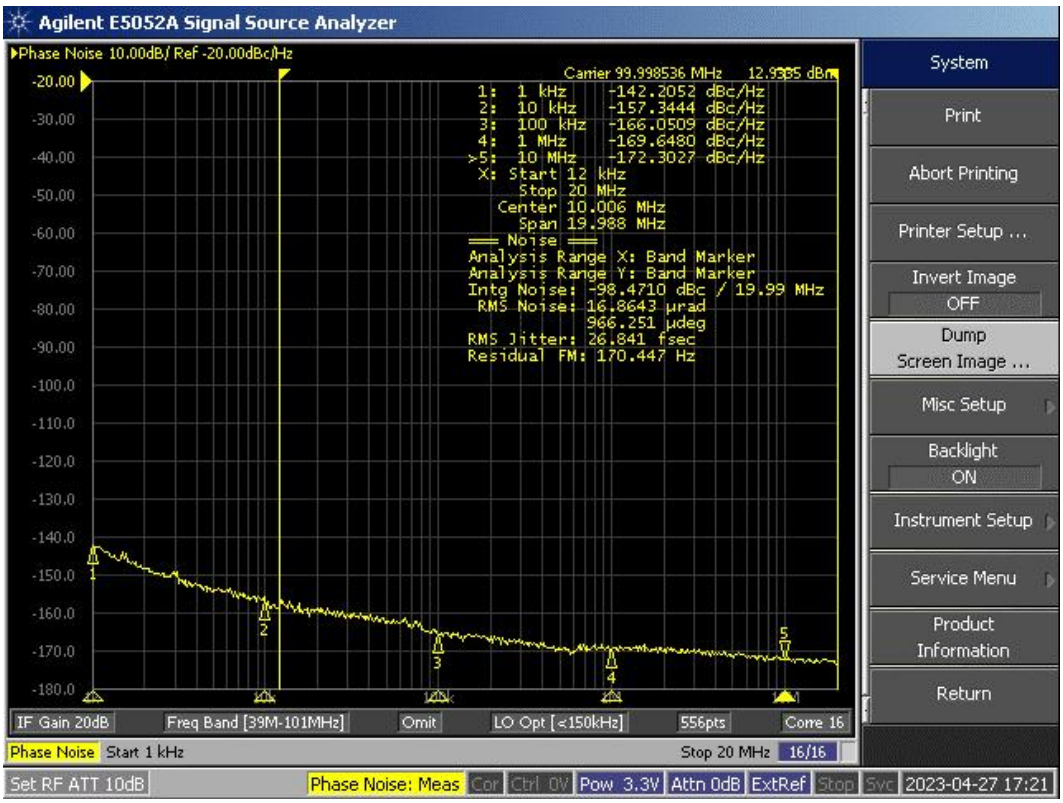


Figure 1

Figure 1 shows the low-noise 100-MHz reference source driving the **YQ1S105** at 3.3-V supply.

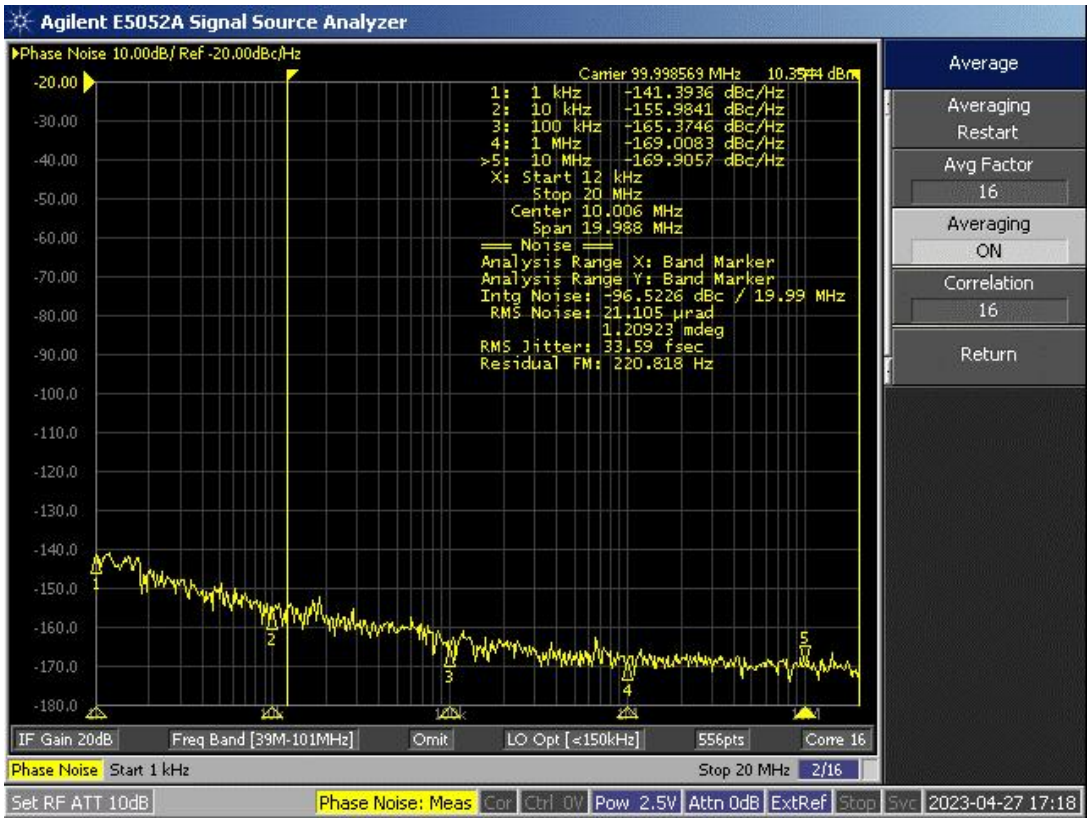


Figure **2**

Figure **2** shows the low-noise 100-MHz reference source driving the **YQ1S105** at 2.5-V supply.

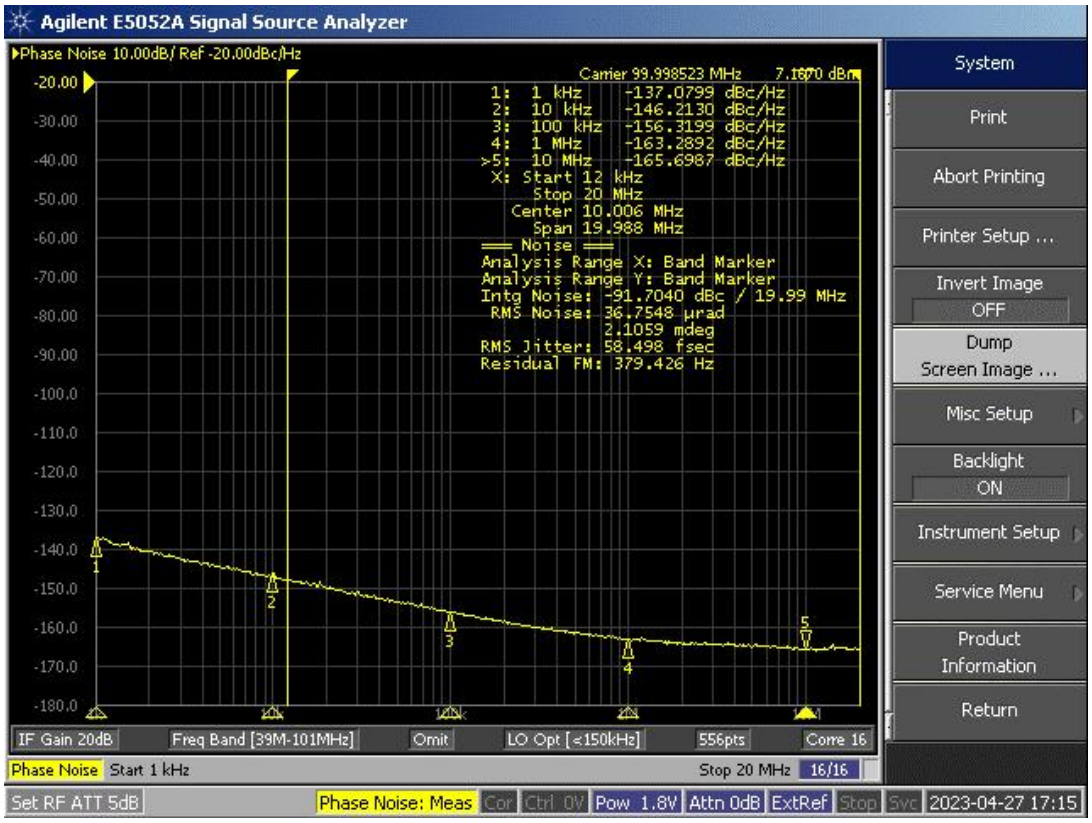


Figure 3

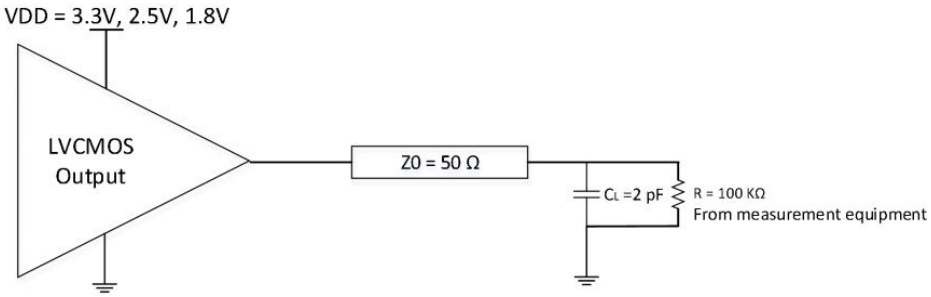
Figure 3 shows the low-noise 100-MHz reference source driving the **YQ1S105** at 1.8-V supply.

Detailed Description

Overview

The YQ1S105 is a 5-output clock fan out buffer with low additive jitter that can operate up to 250 MHz. The device is offered in a 8-pin SOP package. For best signal integrity, it is important to match the characteristic impedance of the YQ1S105's output driver with that of the transmission line.

Parameter Measurement Information



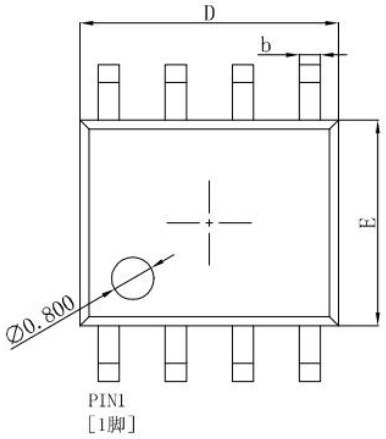
Test Load Circuit

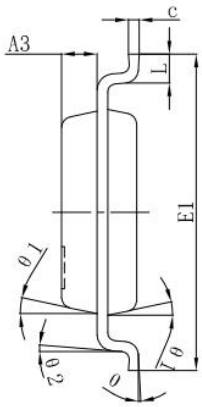
Order Information

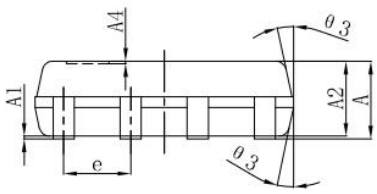
Part No.	Package	Mark	Tape and Reel Information
YQ1S105	SOP-8L		xxxxpcs/Reel

Package Outline

SOP -8L







SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.300	1.500	1.700
A1	0.100	0.150	0.200
A2	1.350	1.420	1.550
A3	0.645	0.670	0.695
A4	0.020	--	0.050
c	0.170	0.203	0.250
E	3.800	3.900	4.000
E1	5.800	6.000	6.200
L	0.450	0.600	0.750
b	0.330	0.400	0.510
D	4.800	4.900	5.000
e	1.270BSC		
θ	0°	3°	8°
θ1	12° REF.		
θ2	5° REF.		
θ3	12° REF.		

Revision History

No	Date	Description
V1.0	202308	First release