DATASHEET

General Description

The YQ1D310 is a 10-output differential high-performance clock buffer.

The input can be selected from two differential inputs or one crystal input. The selected input clock is distributed to two banks of 5 differential outputs and one LVCMOS output. Both differential output banks can be independently configured as LVPECL, LVDS, or HCSL mode, or disabled. The LVCMOS output has a synchronous enable input for glitch-free operation when enabled or disabled.

The device is designed for a signal fanout of high-frequency, low phase-noise clock. It is designed to operate from a 3.3V/2.5V core power supply, and 3 independent output supplies: 3.3V/2.5V.

Applications

- Clock Distribution and Level Translation for ADCs, DACs, Multi-Gigabit Ethernet, XAUI, SATA/SAS, SONET/SDH, CPRI, High Frequency Backplanes
- Switches, Routers, Line Cards, Timing Cards
- Servers, Computing, PCI Express (PCIe 3.0, 4.0)
- Remote Radio Units and Baseband Units
- Test and Measurement

Features

- Two differential reference clock pairs
- Input pairs can accept the following differential input levels: LVPECL, LVDS, HCSL, HSTL or Single Ended
- Crystal Input accepts 10MHz to 100MHz Crystal or Single Ended Clock
- Maximum Output Frequency

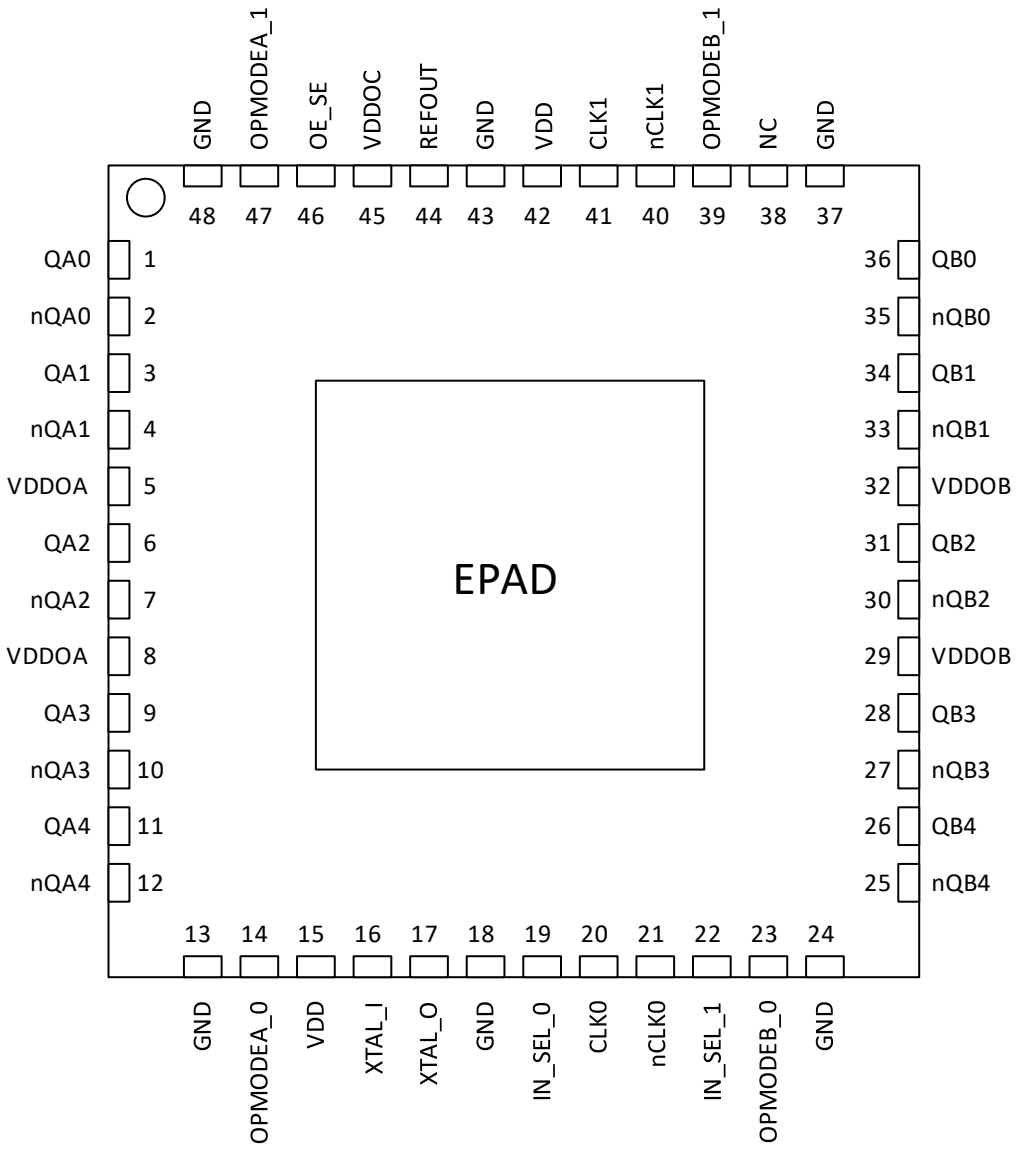
LVPECL	- 2GHz
LVDS	- 2GHz
HCSL	- 350MHz
LVCMOS	- 250MHz

- Two banks, each has five differential output pairs that can be separately configured as LVPECL or LVDS or HCSL or Hi-Z
- One single-ended reference output with synchronous enable to avoid glitch
- Output skew: 30ps (typical)
- Part-to-part skew: 60ps (typical)
- Additive RMS phase jitter @ 156.25MHz: 50 fs RMS (10kHz - 20MHz), @ 3.3V/ 3.3V
- Supply voltage modes:

VDD	VDDO
3.3V	3.3V
3.3V	2.5V
2.5V	2.5V

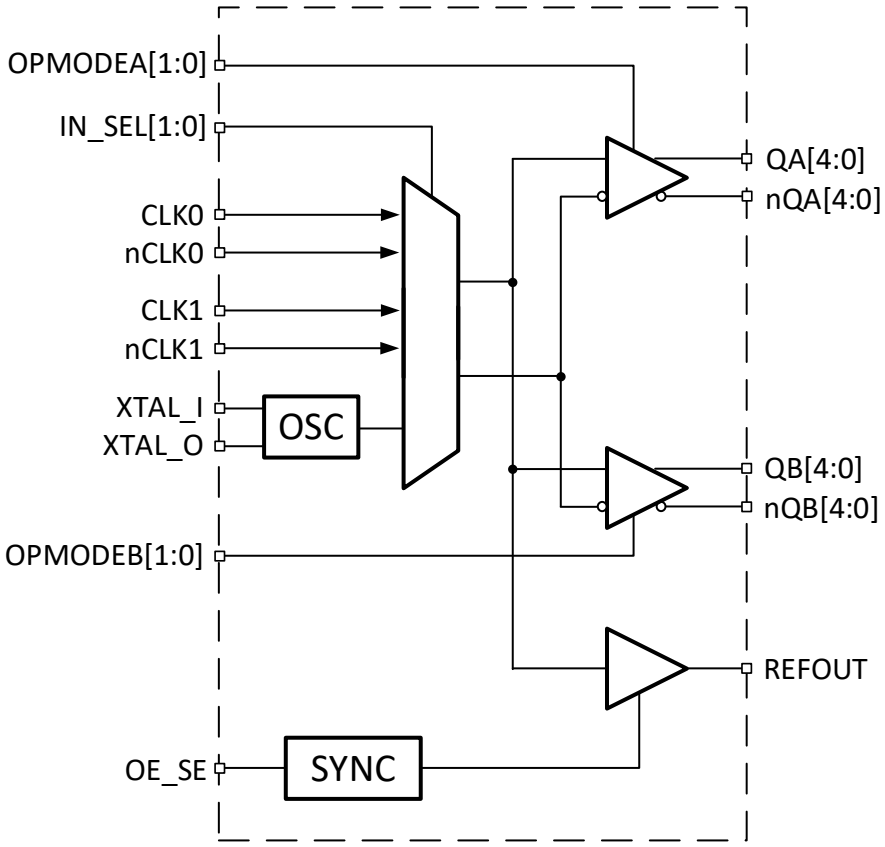
- Industrial Temperature Range: -40°C to 85°C
- Available in 48-pin, 7mm*7mm QFN package

Pin Configuration



48-pin QFN (Top View)

Block Diagram



Pin Descriptions

Number	Name	Type	Description
1	QA0	Output	Bank A differential output pair 0. Pin selectable LVPECL/LVDS/HCSL interface levels.
2	nQA0	Output	Bank A differential output pair 0. Pin selectable LVPECL/LVDS/HCSL interface levels.
3	QA1	Output	Bank A differential output pair 1. Pin selectable LVPECL/LVDS/HCSL interface levels.
4	nQA1	Output	Bank A differential output pair 1. Pin selectable LVPECL/LVDS/HCSL interface levels.
5	VDDOA	Power	Power supply pins for Bank A outputs. 3.3V or 2.5V.
6	QA2	Output	Bank A differential output pair 2. Pin selectable LVPECL/LVDS/HCSL interface levels.
7	nQA2	Output	Bank A differential output pair 2. Pin selectable LVPECL/LVDS/HCSL interface levels.
8	VDDOA	Power	Power supply pins for Bank A outputs. 3.3V or 2.5V.
9	QA3	Output	Bank A differential output pair 3. Pin selectable LVPECL/LVDS/HCSL interface levels.
10	nQA3	Output	Bank A differential output pair 3. Pin selectable LVPECL/LVDS/HCSL interface levels.
11	QA4	Output	Bank A differential output pair 4. Pin selectable LVPECL/LVDS/HCSL interface levels.
12	nQA4	Output	Bank A differential output pair 4. Pin selectable LVPECL/LVDS/HCSL interface levels.
13	GND	Ground	Ground.
14	OPMODEA_0	Input/Pulldown	Output mode select for Bank A. See Table 2 for functions, LVCMOS/LVTTL interface levels.
15	VDD	Power	Power supply pin for Crystal core and input blocks, 3.3V or 2.5V.
16	XTAL_I	Input	Crystal oscillator input pin.

17	XTAL_O	Output	Crystal oscillator output pin.
18	GND	Ground	Ground.
19	IN_SEL_0	Input/Pulldown	Input clock selection. See Table 1 for functions, LVCMOS/LVTTL interface levels.
20	CLK0	Input/Pulldown	Reference input 0. Internally biased to ground.
21	nCLK0	Input/Pullup-Pulldown	Inverting reference input 0. Internally biased to 0.5*VDD.
22	IN_SEL_1	Input/Pulldown	Input clock selection. See Table 1 for functions, LVCMOS/LVTTL interface levels.
23	OPMODEB_0	Input/Pulldown	Output mode select for Bank B. See Table 2 for functions, LVCMOS/LVTTL interface levels.
24	GND	Ground	Ground.
25	nQB4	Output	Bank B differential output pair 4. Pin selectable LVPECL/LVDS/HCSL interface levels.
26	QB4	Output	Bank B differential output pair 4. Pin selectable LVPECL/LVDS/HCSL interface levels.
27	nQB3	Output	Bank B differential output pair 3. Pin selectable LVPECL/LVDS/HCSL interface levels.
28	QB3	Output	Bank B differential output pair 3. Pin selectable LVPECL/LVDS/HCSL interface levels.
29	VDDOB	Power	Power supply pins for Bank B outputs. 3.3V or 2.5V.
30	nQB2	Output	Bank B differential output pair 2. Pin selectable LVPECL/LVDS/HCSL interface levels.
31	QB2	Output	Bank B differential output pair 2. Pin selectable LVPECL/LVDS/HCSL interface levels.
32	VDDOB	Power	Power supply pins for Bank B outputs. 3.3V or 2.5V.
33	nQB1	Output	Bank B differential output pair 1. Pin selectable LVPECL/LVDS/HCSL interface levels.
34	QB1	Output	Bank B differential output pair 1. Pin selectable LVPECL/LVDS/HCSL interface levels.
35	nQB0	Output	Bank B differential output pair 0. Pin selectable LVPECL/LVDS/HCSL interface levels.
36	QB0	Output	Bank B differential output pair 0. Pin selectable LVPECL/LVDS/HCSL interface levels.
37	GND	Ground	Ground.
38	NC	Unused	No connect pin.
39	OPMODEB_1	Input/Pulldown	Output mode select for Bank B. See Table 2 for functions, LVCMOS/LVTTL interface levels.
40	nCLK1	Input/Pull-Pulldown	Inverting reference input 1. Internally biased to 0.5*VDD.
41	CLK1	Input/Pulldown	Reference input 1. Internally biased to ground.
42	VDD	Power	Power supply pin for Crystal core and input blocks, 3.3V or 2.5V.
43	GND	Power	Ground.
44	REFOUT	Output	Single-ended reference clock output. LVCMOS interface levels.
45	VDDOC	Power	Power supply pin for REFOUT output.
46	OE_SE	Input/Pulldown	Synchronous output enable for REFOUT. See Table 3 for functions, LVCMOS/LVTTL interface levels.
47	OPMODEA_1	Input/Pulldown	Output mode select for Bank A. See Table 2 for functions, LVCMOS/LVTTL interface levels.
48	GND	Power	Ground.

Functions Table

Table 1: Input Selection

IN_SEL[1:0]	Selected Input
2'00(default)	CLK0, nCLK0
2'01	CLK1, nCLK1
2'1X	XTAL_I/XTAL_O (Crystal or external clock)

Table 2: Output Mode Selection

OPMODEA/B[1:0]	Output Mode(Bank A or B)
2'b00	LVPECL
2'b01	LVDS
2'b10	HCSL
2'b11	Hi-Z

Table 3: Reference Output Enable

OE_SE	REFOUT Output
0	Hi-Z
1	LVCMOS

Table 4: Input/Output Operation Table, OE_SE

Input Status			Output State
OE_SE	**IN_SEL [1:0]**	**CLKx and nCLKx**	**REFOUT**
0 (default)	Don't care	Don't Care	High Impedance
1	10 or 11	Don't Care	Fanout crystal oscillator
1	00 (default)	CLK0 and nCLK0 are both open circuit	Logic Low
		CLK0 and nCLK0 are tied to ground	Logic Low
		CLK0 is high, nCLK0 is low	Logic High
		CLK0 is low, nCLK0 is high	Logic Low
1	01	CLK1 and nCLK1 are both open circuit	Logic Low
		CLK1 and nCLK1 are tied to ground	Logic Low
		CLK1 is high, nCLK1 is low	Logic High
		CLK1 is low, nCLK1 is high	Logic Low

Table 5: Input/Output Operation Table, OPMODEA/B[1:0]

Input Status			Output State
OPMODEA/B[1:0]	IN_SEL[1:0]	CLKx and nCLKx	QA/B[4:0], nQA/B[4:0]
11	Don't care	Don't Care	High Impedance
00, 01 or 10	10 or 11	Don't Care	Fanout crystal oscillator
00, 01 or 10	00 (default)	CLK0 and nCLK0 are both open circuit	QA/B[4:0] = Low nQA/B[4:0] = High
		CLK0 and nCLK0 are tied to ground	QA/B[4:0] = Low nQA/B[4:0] = High
		CLK0 is high, nCLK0 is low	QA/B[4:0] = High nQA/B[4:0] = Low
		CLK0 is low, nCLK0 is high	QA/B[4:0] = Low nQA/B[4:0] = High
00, 01 or 10	01	CLK1 and nCLK1 are both open circuit	QA/B[4:0] = Low nQA/B[4:0] = High
		CLK1 and nCLK1 are tied to ground	QA/B[4:0] = Low nQA/B[4:0] = High
		CLK1 is high, nCLK1 is low	QA/B[4:0] = High nQA/B[4:0] = Low
		CLK1 is low, nCLK1 is high	QA/B[4:0] = Low nQA/B[4:0] = High

Absolute Maximum Ratings

Stresses greater than these listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

Item	Rating
VDD, VDDOx[1]	-0.5 to 4.6V
V_{IN}	-0.3V to VDDOx[1] + 0.5V
Junction Temperature	125°C
Storage Temperature	-55°C to 150°C

NOTE 1. VDDOx denotes VDDOA, VDDOB and VDDOC.

ESD Ratings

		Max	Unit
V(ESD) Electrostatic discharge	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2023	±5000	V
	Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2022	±2000	

Latch Up

		Max	Unit
Latch up	I-test, JEDEC STD JESD78F.02-2023	±450	mA
	V-test, JEDEC STD JESD78F.02-2023	4.95	V

Power Supply Characteristics Operating Conditions

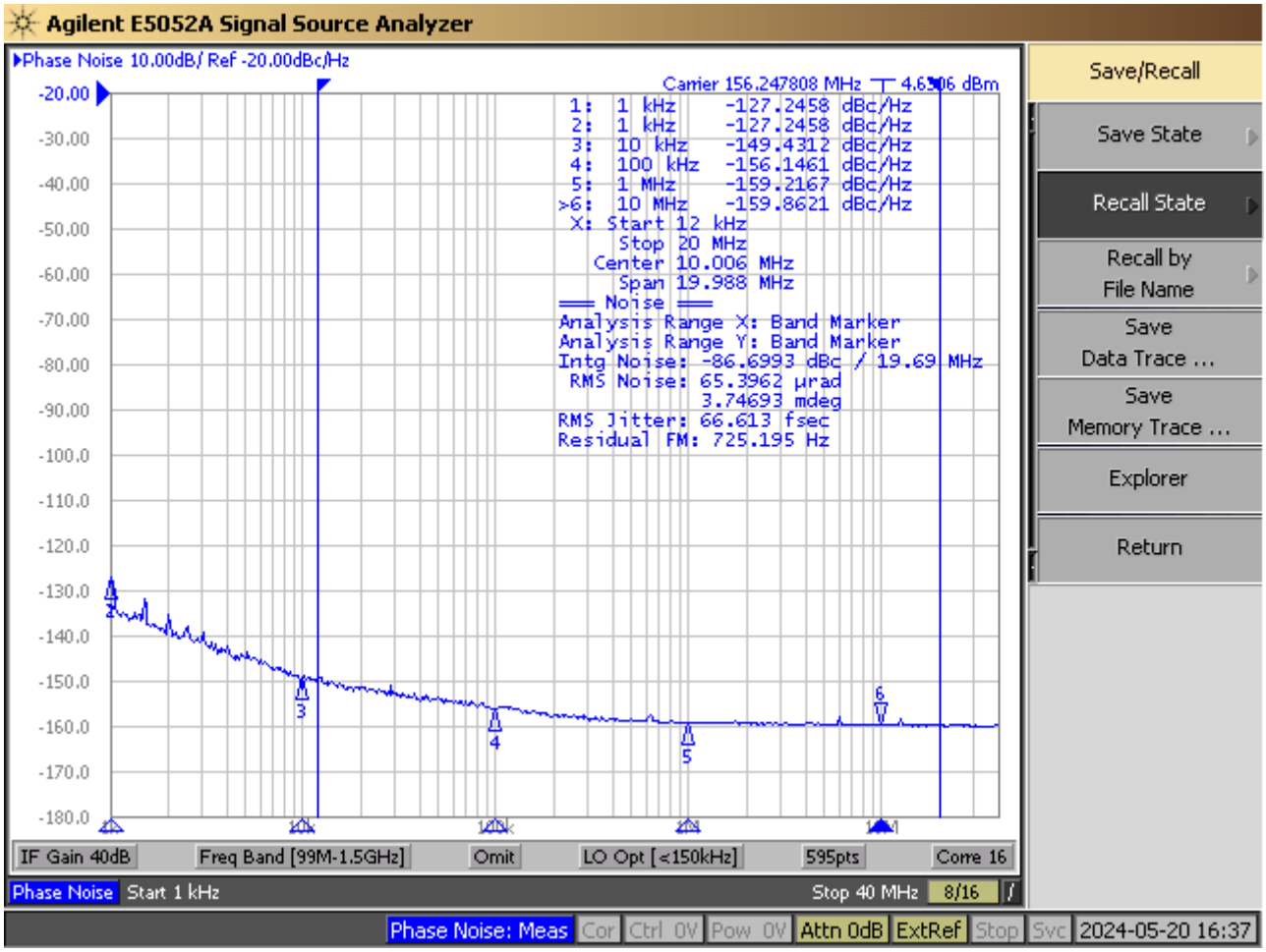
Symbol	Parameter	Min	Typ	Max	Unit
T_A	Ambient air temperature	-40		105	℃
T_J	Junction temperature			125	℃
VDD	Power supply for Crystal core and input blocks	2.375		3.465	V
VDDOx[1]	Power supply for Bank A or B or REFOUT	2.375		3.465	V

NOTE 1. VDDOx denotes VDDOA, VDDOB and VDDOC.

Electrical Characteristics

Additive Phase Jitter

Phase noise, also known as dBc Phase Noise, measures the cleanliness of a frequency band around a central frequency compared to the strength of that central frequency itself. This measurement is typically shown on a phase noise plot, which is commonly used in many technical applications. Phase noise represents the noise power in a 1Hz bandwidth at a certain distance from the central or fundamental frequency, relative to the power of the central frequency. This relationship is expressed in decibels (dBm) or as a ratio of power between the 1Hz band and the fundamental frequency. When a specific offset is defined, this measurement is referred to as a dBc value, indicating dBm at that particular offset. By analyzing jitter through the frequency domain, we gain a clearer insight into its impact on an application across the entire duration of the signal. From a phase noise plot, it is possible to mathematically predict an expected bit error rate.



POWER CONSUMPTION

Parameter		Test Conditions	Min	Typ	Max	Unit
I_{CC_CORE}	Core Supply Current, All Outputs Disabled	CLK0/CLK1 Selected		9		mA
		XTAL_I Selected		11		
I_{CC_PECL}	Additive Core Supply Current, Per VPECL Bank Enabled			34		mA
I_{CC_LVDS}	Additive Core Supply Current, Per LVDS Bank Enabled			41		mA
I_{CC_HCSL}	Additive Core Supply Current, Per HCSL Bank Enabled			16		mA
I_{CC_CMOS}	Additive Core Supply Current, LVCMOS Output Enabled			2		mA
I_{CCO_PECL}	Additive Output Supply Current, Per LVPECL Bank Enabled	Includes Output Bank Bias and Load Currents, R_T = 50 Ω to VDDOx - 2V on all outputs in bank		180		mA
I_{CCO_LVDS}	Additive Output Supply Current, Per LVDS Bank Enabled			40		mA
I_{CCO_HCSL}	Additive Output Supply Current, Per HCSL Bank Enabled			118		mA
I_{CCO_CMOS}	Additive Output Supply Current, LVCMOS Output Enabled	200MHz, $C_L \leq 5$ pF		9		mA

CMOS Control Inputs (IN_SEL[1:0], OPMODEA[1:0], OPMODEB[1:0], OE_SE)

Parameter		Test Conditions	Min	Typ	Max	Unit
V_{IH}	High-Level Input Voltage		1.6		VDD	V
V_{IL}	Low-Level Input Voltage		GND		0.4	V
I_{IH}	High-Level Input Current	V_{IH} = VDD, Internal pulldown resistor			60	uA
I_{IL}	Low-Level Input Current	V_{IL} = 0V, Internal pulldown resistor		0.1		uA

Crystal Oscillator Interface (XTAL_I, XTAL_O)

Parameter		Test Conditions	Min	Typ	Max	Unit
F_{CLK}	External Clock Frequency Range	XTAL_I driven, XTAL_O left floating	1		250	MHz
F_{XTAL}	Crystal Frequency		8		100	MHz
C_{IN}	XTAL_I input Capacitance			2		pF

Clock Inputs (CLK0, nCLK0, CLK1, nCLK1)

Parameter		Test Conditions	Min	Typ	Max	Unit
F_{CLKin}	Input Frequency Range		DC		2000	MHz
V_{IHD}	Differential Input High Voltage	Driven differentially			VDD	V
V_{ILD}	Differential Input Low Voltage		GND			V
V_{ID}	Differential Input Voltage Swing		0.1		1.5	V
V_{CMD}	Differential Input Common Voltage	V_{ID} = 200mV	0.25		VDD-1.2	V
V_{IH}	Singel-ended Input High Voltage	CLKx/nCLKx driven single-ended (AC or DC coupled)			VDD	V
V_{IL}	Singel-ended Input Low Voltage		GND			V
V_{I_SE}	Singel-ended Input Voltage Swing		0.3		2.2	V_{PP}
V_{CM}	Singel-ended Input Common Voltage		0.25		VDD-1.2	V
ISO_{MUX}	Mux Isolation, CLK0 to CLK1	156.25MHz		90		dB

LVPECL OUTPUTS

Parameter		Test Conditions		Min	Typ	Max	Unit
f_{CLKout_FS}	Maximum Output Frequency Full V_{OD} Swing	VOD ≥ 600 mV, RL = 100 Ω differential	VDDO = 3.3 V ± 5%, RT = 160 Ω to GND	1.0			GHz
			VDDO=2.5 V ± 5%, RT = 91 Ω to GND	1.0			
f_{CLKout_RS}	Maximum Output Frequency Reduced V_{OD} Swing	VOD ≥ 400 mV, RL = 100 Ω differential	VDDO = 3.3 V ± 5%, RT = 160 Ω to GND	2.1			GHz
			VDDO=2.5 V ± 5%, RT = 91 Ω to GND	2.0			
$Jitter_{ADD}$	Additive RMS Jitter, Integration Bandwidth 10 kHz to 20MHz	VDDO=3.3 V ± 5%: RT = 160 Ω to GND, RL = 100 Ω differential	CLKin: 156.25 MHz, Slew rate ≥ 3 V/ns	50			fs
Noise Floor	Noise Floor f_{OFFSET} ≥ 10 MHz	VDDO=3.3 V ± 5%: RT = 160 Ω to GND, RL = 100 Ω differential	CLKin: 156.25 MHz, Slew rate ≥ 3 V/ns	-163			dBc/Hz
DUTY	Duty Cycle	50% input clock duty cycle		45%		55%	
V_{OH}	Output High Voltage	T_A = 25 °C, DC Measurement, R_T = 50 Ω to VDDO - 2 V		VDDO - 1.2		VDDO - 0.8	V
V_{OL}	Output Low Voltage			VDDO - 2.0		VDDO - 1.6	V

V_{OD}	Output Voltage Swing		600	800	1000	mV
t_R	Output Rise Time 20% to 80%	R_T = 160 Ω to GND, Uniform transmission line up to 10 in. with 50-Ω characteristic impedance, R_L = 100 Ω differential, C_L ≤ 5 pF		200		ps
t_F	Output Fall Time 80% to 20%			200		ps

LVDS OUTPUTS

Parameter		Test Conditions		Min	Typ	Max	Unit
f_{CLKout_FS}	Maximum Output Frequency Full V_{OD} Swing	V_{OD} ≥ 250 mV, R_L = 100 Ω differential			1.45		GHz
f_{CLKout_RS}	Maximum Output Frequency Reduced V_{OD} Swing	V_{OD} ≥ 200 mV, R_L = 100 Ω differential			2		GHz
$Jitter_{ADD}$	Additive RMS Jitter, Integration Bandwidth 10 kHz to 20 MHz	VDDO = 3.3 V, R_L = 100 Ω differential	CLKin: 156.25 MHz, Slew rate ≥ 3 V/ns		55		fs
Noise Floor	Noise Floor f_{OFFSET} ⩾ 10MHz	VDDO = 3.3 V, R_L = 100 Ω differential	CLKin: 156.25 MHz, Slew rate ≥ 3 V/ns		-160		dBc/Hz
DUTY	Duty Cycle	50% input clock duty cycle		45%		55%	
V_{OD}	Output Voltage Swing	T_A = 25 °C, DC Measurement, R_L = 100 Ω differential		250	350	450	mV
ΔV_{OD}	Change in Magnitude of V_{OD} for Complementary Output States			-35		35	mV
V_{OS}	Output Offset Voltage			1.1	1.25	1.35	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complementary Output States			-30		30	mV
t_R	Output Rise Time 20% to 80%	Uniform transmission line up to 10 inches with 50-Ω characteristic impedance, R_L = 100 Ω differential, C_L ≤ 5 pF			200	400	ps
t_F	Output Fall Time 80% to 20%				200	400	ps

HCSL OUTPUTS

Parameter		Test Conditions		Min	Typ	Max	Unit
f_{CLKout}	Output Frequency Range	R_L = 50 Ω to GND, C_L ≤ 5 pF		DC		350	MHz
$Jitter_{ADD}$	Additive RMS Jitter Integration Bandwidth 1 MHz to 20 MHz	VDDO = 3.3 V, R_T = 50 Ω to GND	CLKin: 156.25 MHz, Slew rate ≥3 V/ns		80		fs
Noise Floor	Noise Floor f_{OFFSET} ≥ 10 MHz	VDDO = 3.3 V, R_T = 50 Ω to GND	CLKin: 156.25 MHz, Slew rate ≥ 3 V/ns		-160		dBc/Hz
DUTY	Duty Cycle	50% input duty cycle		45%		55%	
V_{OH}	Output High Voltage	T_A = 25 °C, DC Measurement, R_T = 50 Ω to GND		700	800	900	mV
V_{OL}	Output Low Voltage			-50	0	50	mV
V_{CROSS}	Absolute Crossing Voltage	R_L = 50 Ω to GND, C_L ≤ 5 pF		200	350	500	mV
ΔV_{CROSS}	Total Variation of V_{CROSS}					100	mV
t_R	Output Rise Time 20% to 80%	350 MHz, Uniform transmission line up to 10 inches with 50-Ω characteristic impedance, R_L = 50 Ω to GND, C_L ≤ 5 pF			300	500	ps
t_F	Output Fall Time 80 % to 20%				300	500	ps

LVCMOS OUTPUTS (REFOUT)

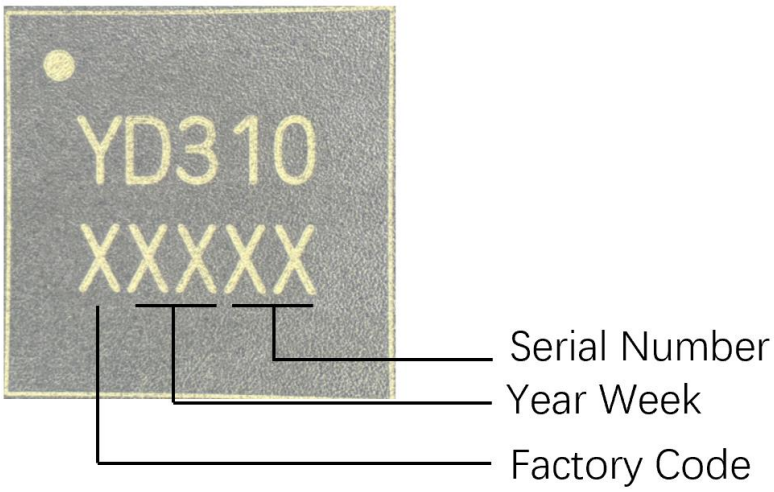
Parameter		Test Conditions		Min	Typ	Max	Unit
f_{CLKout}	Output Frequency Range	C_L ≤ 5 pF		DC		250	MHz
$Jitter_{ADD}$	Additive RMS Jitter Integration Bandwidth 1 MHz to 20 MHz	VDDO = 3.3 V, C_L ≤ 5 p	156.25 MHz, Slew rate ≥3 V/ns		70		fs
Noise Floor	Noise Floor f_{OFFSET} ≥ 10 MHz	VDDO = 3.3 V, R_T = 50 Ω to GND	156.25 MHz, Slew rate ≥ 3 V/ns		-160		dBc/Hz
DUTY	Duty Cycle	50% input duty cycle		45%		55%	
V_{OH}	Output High Voltage	1mA load current		VDDO-0.1			V
V_{OL}	Output Low Voltage					0.1	V
t_R	Output Rise Time 20% to 80%	250 MHz, Uniform transmission line up to 10 inches with 50-Ω characteristic impedance, R_L = 50 Ω to GND, C_L ≤ 5 pF			250		ps
t_F	Output Fall Time 80 % to 20%				250		ps

t_{EN}	Output Enable Time	$C_L \le 5$ pF		2	4	cycles
t_{DIS}	Output Disable Time			2	4	cycles

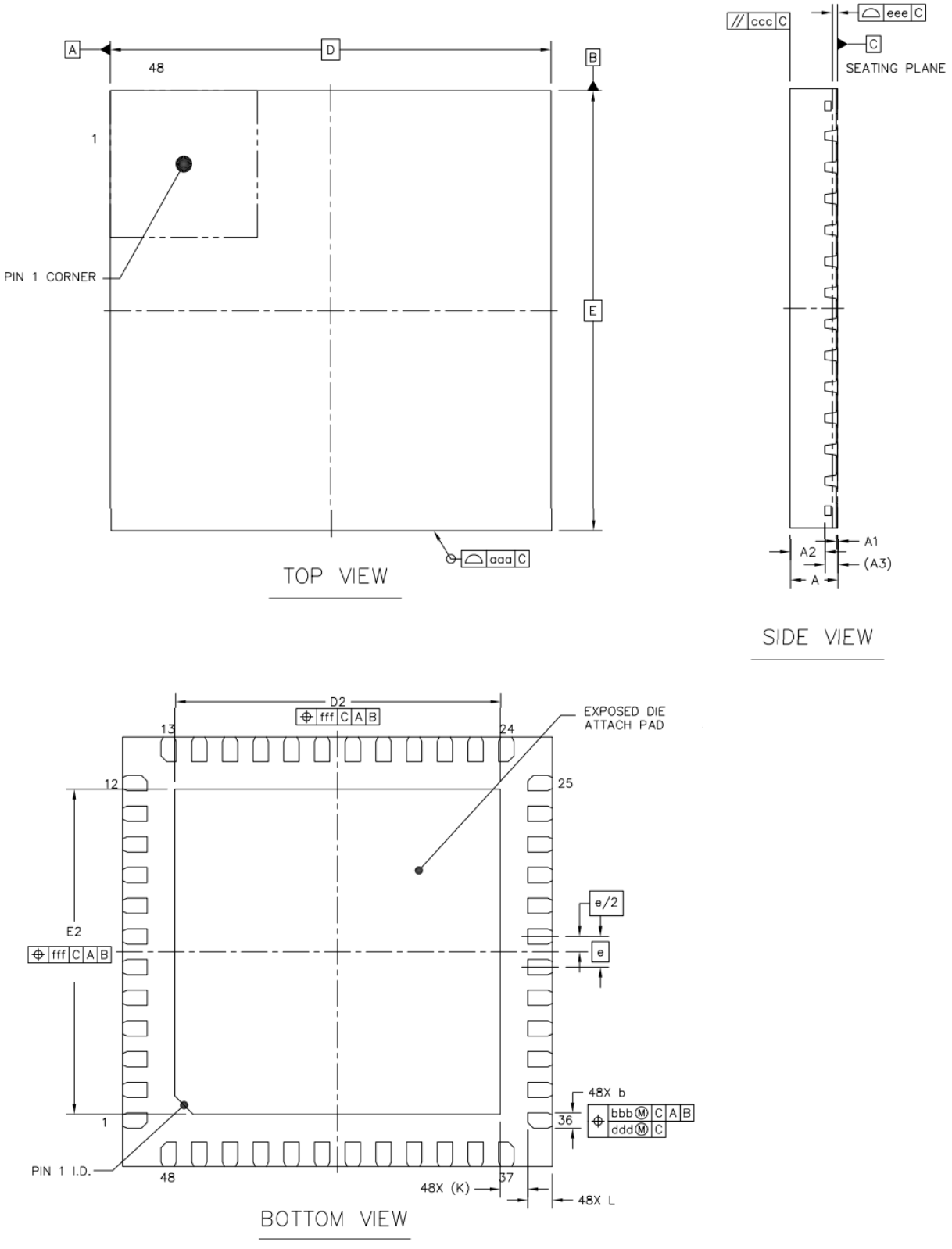
Propagation Delay and Output Skew

Parameter		Test Conditions		Min	Typ	Max	Unit
t_{PD_LVPECL}	Propagation Delay CLKin-to-LVPECL	RT = 160 Ω to GND, RL = 100 Ω differential, $C_L \le 5$ pF			400		ps
t_{PD_LVDS}	Propagation Delay CLKin-to-LVDS	RL = 100 Ω differential, $C_L \le 5$ pF			400		ps
t_{PD_HCSL}	Propagation Delay CLKin-to-HCSL	RL = 100 Ω differential, $C_L \le 5$ pF			550		ps
$t_{SK(O)}$	Output Skew LVPECL/LVDS/HCSL	Skew specified between any two CLKouts with the same buffer type. Load conditions per output type are the same as propagation delay specifications.			30		ps
$t_{SK(PP)}$	Part-to-Part Output Skew LVPECL/LVDS/HCSL				60		ps
t_{PD_CMOS}	Propagation Delay CLKin-to-CMOS	$C_L \le 5$ pF	VDDOC=3.3V		1.5		ns
			VDDOC=2.5V		1.6		

Package Marking



Package Outline



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		7 BSC	
	Y	E		7 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	D2	5.2	5.3	5.4
	Y	E2	5.2	5.3	5.4
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.45 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
		ddd		0.05	
EXPOSED PAD OFFSET		fff		0.1	

NOTES

1.REFER TO JEDEC MO-220;
2.COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD;
3.BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES OF JCET PRESCRIBING;
4.FINISH: Cu/EP •Sn8~20s

Revision History

No	Date	Description
V0.5	2024.04.13	Initial release
V0.9	2024.06.14	Optimize power consumption test result
V1.0	2024.08.12	Add package marking info